

AN ACTIVE-MATRIX BACKPLANE DESIGN USING THE SHADOW- MASK PROCESS TO
CREATE A SYSTEM ON GLASS (SOG) WITH INTEGRATED DRIVERS

Charles Harrigal

ABSTRACT:

Through shadow-masking techniques, we have economically produced active-matrix backplanes with integrated driving circuitry. The TFT's have speeds and currents necessary to drive an E-Paper or OLED front-planes. Additionally, they have leakage currents low enough to have power consumption advantages.

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OBJECTIVE AND BACKGROUND:

The goal of the project was to develop a backplane design that drives e-paper as a front-plane. The device needed to be active-matrix. The backplane requirements were

- to be economical enough to be competitive with existing techniques
- with speeds capable of loading an e-paper page within seconds (3 in our specific case)
- Drive capability of greater than 100 μA .
- Leakage currents below 10 pA .
- Stability of less than 5% drift over 16 hours.

In the past, integrating logic and driving circuits on the backplane substrate have resulted in either poor TFT characteristics or one that makes the manufacturing process not economically feasible. If the TFT's were made by previous thin-film techniques, the parameters were not acceptable for our integrated driving circuits. By using monolithic silicon as a substrate, we would get the performance necessary, but the costs would be increased. Thus, the goal was to enhance the thin-film-transistors parameters without increasing the costs.

METHODS:

In order to keep the cost to a minimum, we restricted the manufacture of the backplane using shadow-masking techniques where possible. Shadow-masking is more cost effective than photolithography. With our shadow-masking techniques, we can obtain 1-micron accuracy. This was one of the key elements to achieving our goals.

A means of reducing costs is to transmit data serially. Thus, this meant that we needed to integrate the driving circuitry on the backplane, thus changing many parallel bits of data to only several serial data bits. This not only reduces the cost of the driving electronics, but also that of the connections.

The task was to develop backplane for a 1.7 x 1.3 inch e-paper display. This gave us approximately 100 dpi (dots per inch), although these techniques can go up to approximately 200 dpi. Thus, we have the flexibility to increase or decrease the display size and resolution

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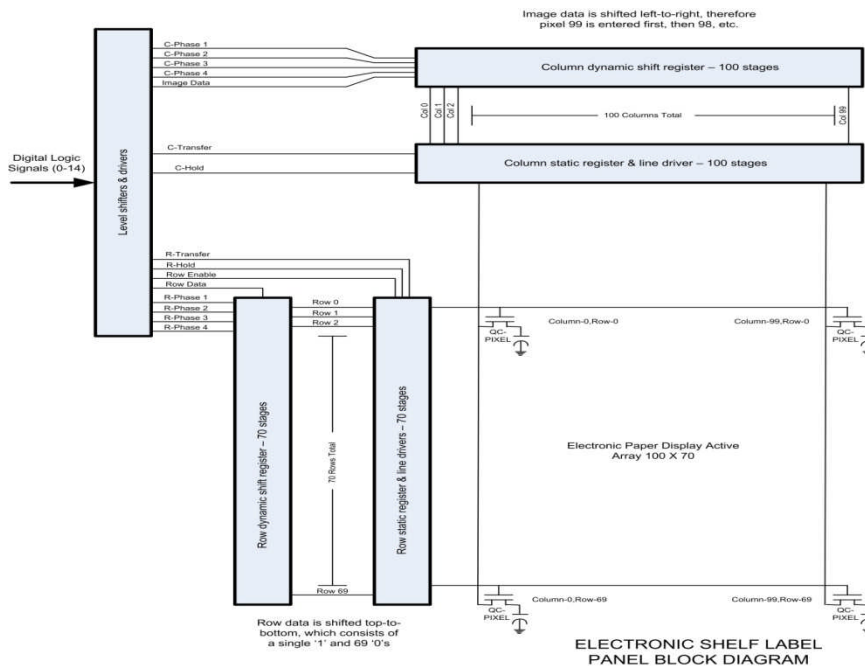
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TFT gate length and widths were controlled to increase the speed and saturation current. We were still able to keep the breakdown voltage to a desirable level. Also, proper thermal annealing achieved stability as well as enhancing TFT performance.

These as well as with some other minor enhancements, we were able to meet our goals for cost and performance.

The driving circuitry was an array of 100 columns by 70 rows. For each row, the data was loaded serially into dynamic pseudo-D shift registers. Then when the entire row's shift registers were loaded, the data is stored into an inverter static memory cell and driven into the pixel array. The rows contain identical driving circuitry; however, the row data is just a leading "1" followed by 69 "0". Thus, data is loaded one row at a time from the top to the bottom of the pixel array. See Figure 1 below for a high-level diagram of the circuitry. Then, Figure 2 has a single driver stage in block form.

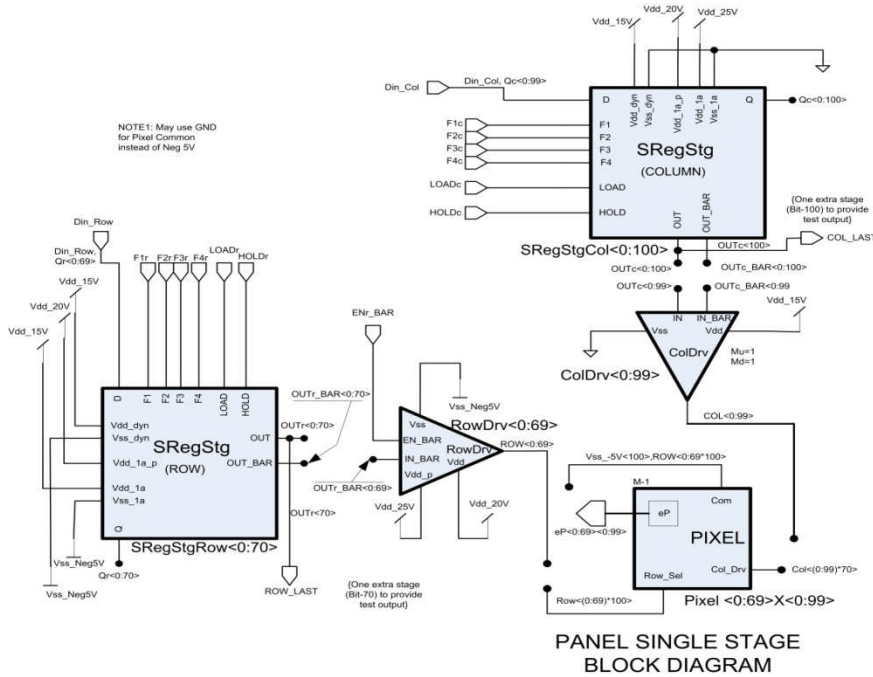
FIGURE 1:



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FIGURE 2:



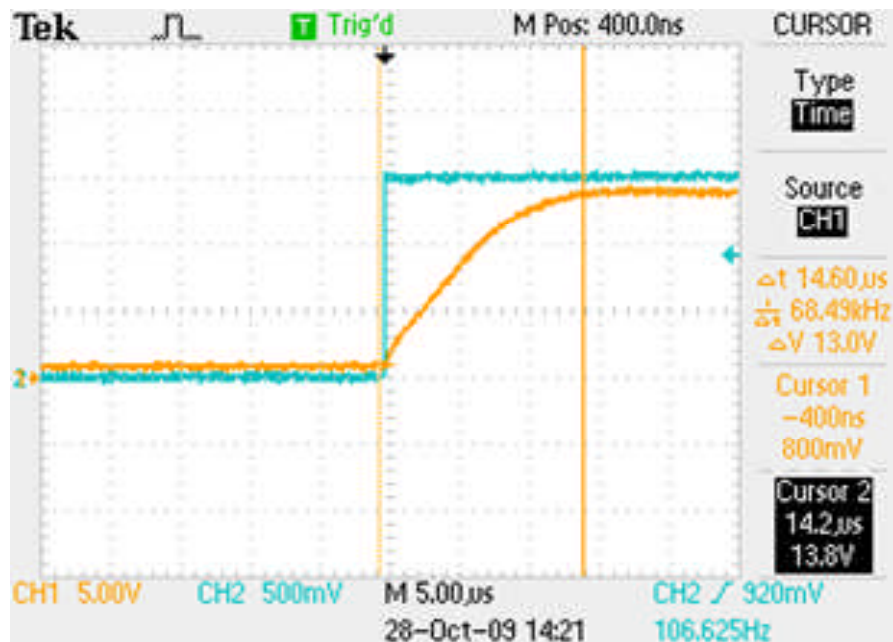
RESULT:

First I will cover performance. The speed of the FET's have increased from before enhancements maximum frequency of 1.5 kHz., to a present speed of 35 kHz. Then for the next version, which will be tested before the end of the 2009, we anticipate a maximum frequency of over 150 kHz. Regardless, it will be faster than the 35 kHz, by more than double. These are speeds faster than we needed for our present project. That is, we needed speeds of 11,667 Hz. in order to accomplish our goal of downloading a page of ESL data within 3 seconds. The oscilloscope picture below will verify the speed. Only rise time is measured at 14 usec. (4 t) but the fall time is identical. This indicates a speed faster than what we need for the above requirement.

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FIGURE 3:

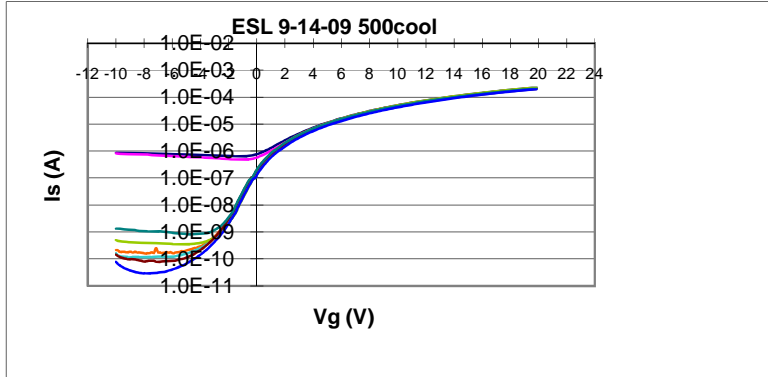


Rapid thermal annealing improves the parameters of the TFT. And saturation current has been improving over the course of the project. We started out obtain saturation currents around 50 ua. Now we are reaching saturation currents of 200 ua. on a consistent basis. Leakage currents have also been improving over the project. We are currently obtaining leakage currents below 10 ua. These observations are illustrated by TFT parameter characteristic curves for a sample of 3 TFT's from a recent backplane as Figure 4.

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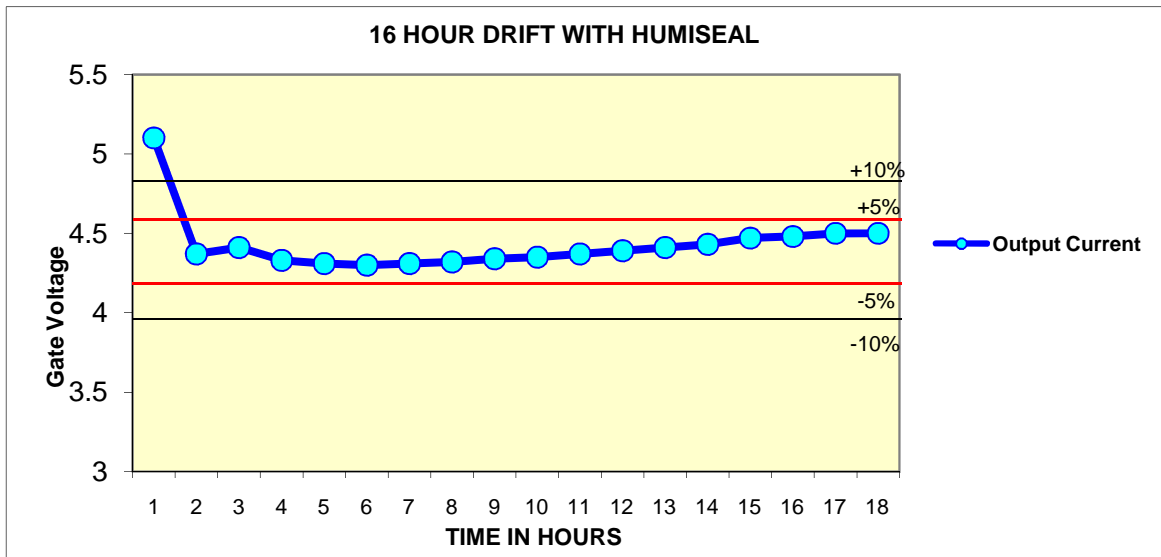
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FIGURE 4:



Drift. The following graph shows variation in leakage current over a 16 hour period.

FIGURE 5



The second part of the paper deals with the economics . The cost advantage of our ESL needs to be proven in a production environment. However in general there is

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a 4 to 1 cost saving of shadow-masking to photolithography. This ESL project requires 6 shadow-masking steps and one photolithography step versus all photolithography. This leads to a 65% savings. In practice on other projects the savings typically is closer to 55%.

REFERENCES: Here are samples of papers that our company's personnel have presented on similar subjects.

T.P. Brody, "The Birth and Early Childhood of Active Matrix – A personal Memoir", Journal of the SID, 4/3, 1996, pp.113-127.

T.P. Brody, et al, "A 6X6 in. 20 lines-per-inch liquid crystal display panel", IEEE Trans Electron Dev 20, 995-1001 (1973).

T P Brody, et al, "A 6X 6 in TFT-addressed electroluminescent display panel," IEDM, Washington, DC (1973); Conf Record, IEEE-SID Conf on Display Devices 1974, pp. 129-131.

PRIOR PUBLICATIONS: This is the first publication on the subject of integrated drivers by Advantech US, Inc. Investigations into publications on integrated drivers did not produce any with similar results.